Amendments to the Specification

Please replace paragraph [0070] of the specification with the following amended paragraph [0070]:

This is not the case, however, when the method is applied to a circuit having nested feedback loops such as 64-to-1 multiplexer loop 400, as illustrated by FIGs. 12-14. As will become apparent to persons skilled in the relevant arts given the description herein, there are several approaches that can be used in applying pipelining and look-ahead in the context of a multiplexer loop. The ~~know~~ known relevant art does not teach or suggest which form of pipelining and look-ahead, if any, will improve the performance of a circuit having nested feedback loops.

Please replace paragraph [0077] of the specification with the following amended paragraph [0077]:

FIG. 14 illustrates a circuit 1400 developed by applying a second form of pipelining and look-ahead to circuit 1200. This form also is not very useful for improving the performance of circuit 1200. This form is also shown so that it can be contrasted with the present invention. The output of circuit 1400 is given ~~by~~ by EQs. 8a and 8b. EQ. 8a is obtained by substituting past iterations of EQ. 6a and EQ. 6c in EQ. 6a.

$$a_n = (A_n a_{n-2} + B_n \overline{a}_{n-2})(E_{n-1} a_{n-2} + F_{n-1} \overline{a}_{n-2}) + (C_n a_{n-2} + D_n \overline{a}_{n-2})(\overline{E}_{n-1} a_{n-2} + \overline{F}_{n-1} \overline{a}_{n-2}) \quad \text{EQ. 8a}$$

$$a_n = \begin{pmatrix} A_n E_{n-1} \\ + C_n \overline{E}_{n-1} \end{pmatrix} a_{n-2} + \begin{pmatrix} B_n F_{n-1} \\ + D_n \overline{F}_{n-1} \end{pmatrix} \overline{a}_{n-2} \quad \text{EQ. 8b}$$